PRL

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/287,304	04/07/1999	AKIRA YAMAMOTO	0941.63012	6149

24978 7590 02/11/2003

GREER, BURNS & CRAIN
300 S WACKER DR
25TH FLOOR
CHICAGO, IL 60606

EXAMINER
PIZIALI, JEFFREY J

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 02/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

Office Action Summary	Application No. 09/287,304	Applicant(s) YAMAMOTO ET AL.	
	Examiner Jeff Piziali	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *21 November 2001* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 14, 2002 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Youn (US 5,856,816).

Regarding claim 1, Youn discloses a liquid crystal display device including a data driver [Fig. 3] and a gate driver [Fig. 2, 3], comprising an LCD panel [Fig. 2, 1]; a substrate on which the LCD panel, the data driver and the gate driver are integrally formed; the data driver being divided into a plurality of blocks [Fig. 2; D_1-$D2_{n-1}$ & D_2-D_{2n}] so as to divide the LCD panel into sections arranged side by side, which simultaneously supply the LCD panel with display signals respectively supplied thereto; wherein each of the blocks includes a plurality of signal lines [Fig.

3; DA, DB, & DC] that are connected to a plurality of data bus lines [Fig. 3, Data Latch output lines] via a switching device [Fig. 3, 12], a number of the data bus lines being larger than a number of the signal lines, the display signals being supplied from the signal lines of each block to the data bus lines simultaneously, and the blocks are arranged adjacent to each other along a single edge of the LCD panel (Column 1, Line 10 - Column 2, Line 20). Youn does not expressly disclose using analog switches as the switching device.

However, the use of analog switches as switching devices was well known and commonly understood in the art of data latching at the time of invention. Therefore, it would have been obvious to one skilled in the art at the time of invention to using analog switches as Youn's switching device, so as to manufacture the device with commonly available circuitry.

Regarding claim 2, Youn discloses a block comprising a shift register [Fig. 5, 21]; signal lines [Fig. 5, Y] to which the display signals are supplied; data bus lines connected to the signal lines and the LCD panel; and analog switches [Fig. 5, 29-30] provided in the data bus lines and controlled by an output signal of the shift register thereto (Column 4, Line 39 - Column 5, Line 38).

Regarding claim 3, Youn discloses a driver device [Fig. 5, 22-23] which receives display data [Fig. 5, D] externally supplied and outputs the display signals derived therefrom to the blocks of the data driver (Column 4, Line 39 - Column 5, Line 21).

Regarding claim 4, Youn discloses a plurality of driver devices [Fig. 5, 22-23] which are respectively associated with a plurality of ones of the blocks, each of the plurality of driver

devices receiving display data [Fig. 5, D] externally supplied and outputting the display signals derived therefrom to associated blocks of the data driver (Column 4, Line 39 - Column 5, Line 38).

Regarding claim 5, Youn discloses the display signal lines of the associated blocks have parts extending from one of the plurality of driver devices through a space located between the associated blocks [Fig. 5].

Regarding claim 6, Youn discloses a substrate on which the LCD panel, data driver and gate driver are integrally formed (Column 1, Lines 10-20).

Regarding claim 7, Youn discloses the data driver comprises polysilicon transistors (Column 1, Lines 10-20).

Regarding claim 8, Youn discloses a display signal supply device [Fig. 5, 22-23] which outputs the display data [Fig. 5, D] to the driver device (Column 4, Line 39 - Column 5, Line 21).

Regarding claim 9, Youn discloses the display signal display device is formed on the LCD panel (Fig. 1; Column 1, Line 10 - Column 2, Line 20).

Regarding claim 10, Youn discloses a display signal supply device [Fig. 5, 22-23] which outputs the display data [Fig. 5, D] to the plurality of driver devices (Column 4, Line 39 - Column 5, Line 21).

Regarding claim 11, Youn discloses each of the plurality of blocks supplies the LCD panel with a given number of display signals at once (Column 4, Line 39 - Column 5, Line 38).

Regarding claim 12, Youn discloses the driver device comprises a shift register [Fig. 5, 21] which outputs a shift signal, first latch circuits [Fig. 5, 22-23] which latch the display data in response to the shift signal, and second latch circuits [Fig. 5, 25-26] which latch the display data from the first latch circuits in response to a latch enable signal externally supplied (Column 4, Line 39 - Column 5, Line 38).

Regarding claim 13, Youn discloses digital-to-analog converters [Fig. 5, 27-28] which convert the display data from the second latch circuits into analog signals (Column 5, Lines 4-13).

Regarding claim 14, Youn discloses a liquid crystal display device including a data driver [Fig. 3] and a gate driver [Fig. 2, 3], comprising an LCD panel [Fig. 2, 1]; and groups of signal lines [Fig. 2, D_n] for carrying display signals, the signal lines within each of the groups being adjacent to each other along a single edge of the LCD panel, and the data driver being divided into a plurality of adjacently arranged blocks [Fig. 2, D_1-D_{2n-1} & D_2-D_{2n}] from which the groups of signal lines extend over corresponding partial areas of the LCD device so that each of the

groups of signal lines is associated with a respective one of the blocks of the data driver, wherein the signal lines [Fig. 3; DA, DB, & DC] in each of the blocks are connected to a plurality of data bus lines [Fig. 3, Data Latch output lines] via a switching device [Fig. 3, 12], a number of the data bus lines is larger than a number of the signal lines, and the display signal are supplied from the signal lines of each block to the data bus lines simultaneously (Column 1, Line 10 - Column 2, Line 20). Youn does not expressly disclose using analog switches as the switching device.

However, the use of analog switches as switching devices was well known and commonly understood in the art of data latching at the time of invention. Therefore, it would have been obvious to one skilled in the art at the time of invention to using analog switches as Youn's switching device, so as to manufacture the device with commonly available circuitry.

Regarding claim 15, Youn discloses a liquid crystal display device including a data driver [Fig. 3] and a gate driver [Fig. 2, 3], comprising an LCD panel [Fig. 2, 1]; signal lines extending from the data driver [Fig. 2, D_n] and carrying display signals, the data driver and the signal lines being divided into a plurality of blocks [Fig. 2, D_1-D_{2n-1} & D_2-D_{2n}] so that the divided signal lines extending from one of the plurality of blocks extends over a corresponding divided area of the LCD device; the divided signal lines [Fig. 3; DA, DB, & DC] in each of the plurality of blocks being adjacent to each other along a single edge of the LCD panel, said divided signal lines in each of the plurality of blocks are connected to a plurality of data bus lines [Fig. 3, Data Latch output lines] via a switching device [Fig. 3, 12], a number of the data bus lines being larger than a number of the signal lines, and display signals being supplied from the signal lines of each of the blocks to the data bus lines simultaneously (Column 1, Line 10 - Column 2, Line 20). Youn does not expressly disclose using analog switches as the switching device.

However, the use of analog switches as switching devices was well known and commonly understood in the art of data latching at the time of invention. Therefore, it would have been obvious to one skilled in the art at the time of invention to using analog switches as Youn's switching device, so as to manufacture the device with commonly available circuitry.

Regarding claim 16, Youn discloses a liquid crystal display device including a data driver [Fig. 3] and a gate driver [Fig. 2, 3], comprising an LCD panel [Fig. 2, 1]; a substrate on which the LCD panel, the data driver and the gate driver are integrally formed; the data driver being divided into a plurality of blocks [Fig. 2, D_1-D_{2n-1} & D_2-D_{2n}] arranged side by side along a single edge of the LCD panel, and each of the blocks has a plurality of signal lines [Fig. 3; DA, DB, & DC] that extend into the liquid crystal display device and are connected to a plurality of data bus lines [Fig. 3, Data Latch output lines] via a switching device [Fig. 3, 12], a number of the data bus lines being larger than a number of the signal lines, and display signals being supplied from the signal lines of each block to the data bus lines simultaneously (Column 1, Line 10 - Column 2, Line 20). Youn does not expressly disclose using analog switches as the switching device.

However, the use of analog switches as switching devices was well known and commonly understood in the art of data latching at the time of invention. Therefore, it would have been obvious to one skilled in the art at the time of invention to using analog switches as Youn's switching device, so as to manufacture the device with commonly available circuitry.

Regarding claim 17, Youn discloses the data driver comprises polysilicon transistors (Column 1, Lines 10-20).

Response to Arguments

4. Applicants' arguments filed October 14, 2002 have been fully considered, but they are not persuasive. The applicants contend Youn (US 5,856,816) does not disclose a data driver featuring a plurality of blocks arranged side by side, adjacent to each other, and along a single edge. However, the examiner respectfully disagrees. Youn teaches a data driver [Fig. 2, 2a & 2b] being divided into blocks [Fig. 2, D_1-D_{2n}] which drive odd data lines [Fig. 2; D_1, D3, ..., $D2_{n-1}$] and even data lines [Fig. 2; D_2, D_4, ..., D_{2n}] respectively. Along the top-edge of Youn's LCD panel [Fig. 2, 1], odd-numbered data lines [Fig. 2; D_1, D3, ..., $D2_{n-1}$] are arranged adjacent to each other. Along the bottom-edge of the same LCD panel, even-numbered data lines [Fig. 2; D_2, D_4, ..., D_{2n}] are arranged adjacent to each other. The examiner confesses that the odd data lines are not adjacent to one another within the LCD panel itself. Likewise, the even data lines are not adjacent to one another within the LCD panel. However, respectively along the top and bottom edges of the LCD panel, the odd data lines and the even data lines are arranged directly adjacent to each other. The examiner additionally notes that the top and bottom edges comprise two separate and distinct edges of the LCD panel. However, pending claim language only necessitates that each block's signal lines be adjacently arranged along a single edge -- not that such an edge must be commonly shared by all the blocks.

The applicants further contend Youn fails to disclose display signals being supplied from the signal lines of each block to the data bus lines simultaneously. However, the examiner again

respectfully disagrees. Youn teaches display signals [Fig. 3; DA, DB, & DC] being supplied from the signal lines of each block to the data bus lines [Fig. 3, Data Latch output lines] simultaneously -- whereby Youn's data latch [Fig. 3, 12] latches and outputs all three display data signals by means of a single source clock [Fig. 3, SCL] (see Column 1, Line 10 - Column 2, Line 20). By such reasoning, the rejection of the claims is deemed proper and thereby maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

J.P.
February 6, 2003

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600